AMENDMENT

Please amend the claims as follows:

Please cancel claims 1-39.

Please add new claims 44-83.

44. A memory element, comprising:

a conductive layer;

a first dielectric material and a second dielectric material, at least a portion of said conductive layer disposed between said first and second dielectric materials wherein an edge portion of said conductive layer is exposed; and

a programmable resistance material adjacent to said exposed edge portion.

45. The memory element of claim 44, wherein said first dielectric material includes a sidewall surface formed therein, said conductive layer being disposed on said sidewall surface.

46. The memory element of claim 44, wherein said edge portion is an annular contact or a linear contact.

47. The memory element of claim 44, wherein said edge portion encircles at least a portion of said programmable resistance material.

48. The memory element of claim 44, wherein said conductive layer is cup-shaped, said cup-shaped conductive layer having an open end adjacent to said programmable resistance material.

49. The memory element of claim 44, wherein said programmable resistance material comprises a phase-change material.

50. The memory element of claim 44, wherein said programmable resistance material comprises a chalcogen element.

51. A memory element, comprising:

a conductive layer;

a first dielectric material and a second dielectric material, at least a portion of said conductive layer disposed between first and second dielectric materials

wherein an edge portion of said conductive layer is exposed; and

a programmable resistance material in electrical communication with said conductive layer, substantially all of said communication occurring through said exposed edge portion.

52. The memory element of claim 51, wherein said first dielectric material includes a sidewall surface formed therein, said conductive layer being disposed on said sidewall surface.

53. The memory element of claim 51, wherein said edge portion is an annular contact or a linear contact.

54. The memory element of claim 51, wherein said edge portion encircles at least a portion of said programmable resistance material.

55. The memory element of claim 51, wherein said conductive layer is cup-shaped, said cup-shaped conductive layer having an open end adjacent to said programmable resistance material.

56. The memory element of claim 51, wherein said programmable resistance material comprises a phase-change material.

57. The memory element of claim 51, wherein said programmable resistance material comprises a chalcogen element.

58. A memory element, comprising:

a first dielectric material;

a conductive layer disposed on said first dielectric material;

a second dielectric material disposed on said conductive layer wherein an edge portion of said conductive layer is exposed; and

a programmable resistance material adjacent to said edge portion.

59. The memory element of claim 58, wherein said first dielectric material includes a sidewall surface formed therein, said conductive layer being disposed on said sidewall surface.

60. The memory element of claim 58, wherein said edge portion is a linear contact or an annular contact.

61. The memory element of claim 58, wherein said edge portion encircles at least a portion of said programmable resistance material.

62. The memory element of claim 58, wherein said conductive layer is cup-shaped, said cup-shaped conductive layer having an open end adjacent to said programmable resistance material.

63. The memory element of claim 58, wherein said programmable resistance material comprises a phase-change material.

64. The memory element of claim 58, wherein said programmable resistance material comprises a chalcogen element.

65. A memory element, comprising:

a first dielectric material;

a conductive layer disposed on said first dielectric material;

a second dielectric material disposed on said conductive layer wherein an edge portion of said conductive layer is exposed; and

a programmable resistance material in electrical communication with said conductive layer, substantially all of said communication occurring through said exposed edge portion.

66. The memory element of claim 65, wherein said first dielectric material includes a sidewall surface formed therein, said conductive layer disposed on said sidewall surface.

67. The memory element of claim 65, wherein said edge portion is an annular contact or a linear contact.

68. The memory element of claim 65, wherein said edge portion encircles at least a portion of said programmable resistance material.

69. The memory element of claim 65, wherein said conductive layer is cup-shaped, said cup-shaped conductive layer having an open end adjacent to said programmable resistance material.

70. The memory element of claim 65, wherein said programmable resistance material comprises a phase-change material.

71. The memory element of claim 65, wherein said programmable resistance material comprises a chalcogen element.

72. A memory element, comprising:

a first dielectric material having a sidewall surface formed therein;

a conductive sidewall spacer disposed on said sidewall surface;

a second dielectric material disposed on said conductive sidewall spacer wherein an edge portion of said spacer is exposed; and

a programmable resistance material adjacent to said edge portion.

73. The memory element of claim 72, wherein said conductive sidewall spacer comprises at least a first and a second conductive layer, said first conductive layer disposed on

said sidewall surface and said second conductive layer disposed on said first conductive layer.

74. The memory element of claim 73, wherein the resistivity of said first conductive layer is less than the resistivity of said second conductive layer.

75. The memory element of claim 72, wherein said edge portion is an annular contact or a linear contact.

A1 B

76. The memory element of claim 72, wherein said programmable resistance material comprises a phase-change material.

77. The memory element of claim 72, wherein said programmable resistance material comprises a chalcogen element.

78. A memory element, comprising:

a first dielectric material having a sidewall surface formed therein;

a conductive sidewall spacer disposed on said sidewall surface;

a second dielectric material disposed on said conductive sidewall spacer wherein an edge portion of said spacer is exposed; and

a programmable resistance material is electrical communication with said spacer, substantially all of said communication occurring through said exposed edge portion.

79. The memory element of claim 78, wherein said conductive sidewall spacer comprises at least a first and a second conductive layer, said first conductive layer disposed on said sidewall surface and said second conductive layer disposed on said first conductive layer.

80. The memory element of claim 79, wherein the resistivity of said first conductive layer is less than the resistivity of said second conductive layer.

81. The memory element of claim 79, wherein said edge portion is an annular contact or a linear contact.

82. The memory element of claim 79, wherein said programmable resistance material comprises a phase-change material.